

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	09/769954
Filing Date	January 25, 2001
First Named Inventor	Rumynin, Dmitriy
Group Art Unit	2124
Examiner Name	Malzahn, David

Sheet 1 of 1

Attorney Docket No: 1365.039US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
SA	US-5,497,342	03/05/1996	Mou, , et al.	364	786	11/09/1994

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
SA		GOTO, et al., "A 54 x 54-b Regularly Structured Tree Multiplier", <u>IEEE Journal of Solid-State Circuits</u> , Vol 27, No. 9, (Sept. 1992),1229-1236	
SA		HEKSTRA, et al., "A Fast Parallel Multiplier Architecture", <u>IEEE International Symposium on Circuits and Systems</u> , Institute of Electrical and Electronic Engineers, c1977-c1996, 20v. :ill. :28cm, (1992),2128-2131	

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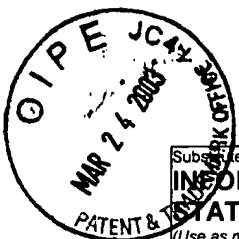
D. H. Malzahn

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12/4/03

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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional) <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached



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Examiner Name	Unknown

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## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
<del>SA</del>	EP-0442356	08/21/1991	Chang, Yen C.	—	—	
<del>SA</del>	WO-99/22292	05/06/1999	Verbauwhede, Ingrid	—	—	

## OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
<del>SA</del>		OKLOBDZIJA, V G., et al., "Improving multiplier design by using improved column compression tree and optimized final adder in CMOS technology", <u>IEEE transactions on Very Large Scale Integration (VLSI) Systems</u> , IEEE, Inc, New York, vol. 3, no. 2, (June 1995), 292-301	
<del>SA</del>		ZURAS, D, et al., "Balanced delay trees and combinatorial division in VLSI", <u>IEEE Journal of Solid State Circuits</u> , IEEE Inc, New York, Vol. SC-21, no. 5, (October 1986), 814-819	

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